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WPI ACC NO: 1990-218408/
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Microcode controller using programmable logic array circuit - has firmware base which allows mainline program to be interrupted and logic nested
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: CONCHA F; LOFFREDO J M
Patent Family (7 patents, 3 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
EP 377976	A	19900718	EP 1989313061	A	19891213	199029 B
CA 2006243	A	19900712				199039 E
US 5043879	A	19910827	US 1989296168	A	19890112	199137 E
EP 377976	A3	19930127	EP 1989313061	A	19891213	199347 E
CA 2006243	C	19940315	CA 2006243	A	19891220	199416 E
EP 377976	B1	19960717	EP 1989313061	A	19891213	199633 E
DE 68926851	E	19960822	DE 68926851	A	19891213	199639 E
			EP 1989313061	A	19891213	

Priority Applications (no., kind, date): US 1989296168 A 19890112
Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 377976	A	EN			
Regional Designated States,Original: DE FR GB					
CA 2006243	A	EN			
EP 377976	A3	EN			
CA 2006243	C	EN			
EP 377976	B1	EN	16	6	
Regional Designated States,Original: DE FR GB					
DE 68926851	E	DE			Application EP 1989313061
					Based on OPI patent EP 377976

Alerting Abstract EP A
The control apparatus uses program logic array circuits. A firmware structure containing a mainline programmable logic array circuit may be used to provide for efficient use of computer micro-codes. As the states of the mainline logic array are sequenced, the data bits representing the encode number field in its OR array are compared with the data bits representing the encode number field of the AND array of the subroutine programmable logic array circuit.

If a match is made, the mainline programmable logic array circuit suspends its operation and sequencing of the subroutine logical array circuit begins in order to perform the function required. Upon completion of the function, control is automatically transferred from the subroutine logical array circuit back to the mainline programmable logic array circuit

at the point where it was suspended. By nesting programmable logic array circuits many functions can take place.
ADVANTAGE - Computer microcode is efficiently used.

Equivalent Alerting Abstract US A
A firmware structure containing a mainline programmable logic array circuit and at least one subroutine programmable logic array circuit may be used. As the states of the mainline programmable logic array circuit are sequenced, the data bits representing the encode number field in its OR array are compared with the data bits representing the encode number field of the AND array of the subroutine programmable logic array circuit. if a match is made, the mainline programmable logic array circuit suspends its operation and sequencing of the subroutine programmable logic array circuit begins, in order to perform the function required. Upon completion of the function, control is automatically transferred from the subroutine programmable logic array circuit back to the mainline programmable logic array circuit, at the point where it was suspended. By nesting a number of subroutine programmable logic array circuits, a number of functions, many of which may be performed simultaneously, can take place.
ADVANTAGE - Efficient use of computer microcodes.
ADVANTAGE - (14pp)

Title Terms /Index Terms/Additional Words: CONTROL; PROGRAM; LOGIC; ARRAY; CIRCUIT; FIRMWARE; BASE; ALLOW; INTERRUPT; NEST

Class Codes
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(Additional/Secondary): B06F-009/22, G06F-001/00
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Canada
Publication No. CA 2006243 A (Update 199039 E)
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Publication Date: 19940315
Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: CONCHA F
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Language: EN
Application: CA 2006243 A 19891220 (Local application)
Priority: US 1989296168 A 19890112
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Germany
Publication No. DE 68926851 E (Update 199639 E)
Publication Date: 19960822
Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: CONCHA F
LOFFREDO J M
Language: DE
Application: DE 68926851 A 19891213 (Local application)
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Priority: US 1989296168 A 19890112
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Original IPC: G06F-9/22(A)
Current IPC: G06F-9/22(A)

EPO
Publication No. EP 377976 A (Update 199029 B)
Publication Date: 19900718
**Mikroprogrammierte Steuervorrichtung mit programmierbaren logischen Anordnungen
Microcode control apparatus utilizing programmable logic array circuits
Dispositif de commande microprogramme utilisant des circuits a reseaux logiques programmables**
Assignee: International Business Machines Corporation, Old Orchard Road, Armonk, N.Y. 10504, US (IBMC)
Inventor: Concha, Fernando, 9604 Saddlebrook Drive, Boca Raton Florida 33496, US
Loffredo, John Mario, 2694 S.W. 14th Drive, Deerfield Beach Florida 33442, US
Agent: Burt, Roger James, Dr., IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, GB
Language: EN
Application: EP 1989313061 A 19891213 (Local application)
Priority: US 1989296168 A 19890112
Designated States: (Regional Original) DE FR GB
Original IPC: B06F-9/22 G06F-1/00 G06F-9/22
Current IPC: B06F-9/22 G06F-1/00 G06F-9/22
Original Abstract: A microcode control apparatus utilizing program logic array circuits is described. A firmware structure containing a mainline programmable logic array circuit and at least one subroutine programmable logic array circuit may be used to provide for efficient use of computer microcodes. As the states of the mainline programmable logic array circuit are sequenced, the data bits representing the encode number field in its OR array are compared with the data bits representing the encode number field of the AND array of the subroutine programmable logic array circuit. If a match is made, the mainline programmable logic array circuit suspends its operation and sequencing of the subroutine programmable logic array circuit begins, in order to perform the function required. Upon completion of the function,control is automatically transferred from the subroutine programmable logic array circuit back to the mainline programmable logic array circuit, at the point where it was suspended. By nesting a plurality of subroutine programmable logic array circuits, a plurality of functions, many of which may be performed simultaneously, can take place.
Claim: The control apparatus uses program logic array circuits. A firmware structure containing a mainline programmable logic array circuit may be

used to provide for efficient use of computer micro-codes. As the states of the mainline logic array are sequenced, the data bits representing the encode number field in its OR array are compared with the data bits representing the encode number field of the AND array of the subroutine programmable logic array circuit.
If a match is made, the mainline programmable logic array circuit suspends its operation and sequencing of the subroutine logical array circuit begins in order to perform the function required. Upon completion of the function, control is automatically transferred from the subroutine logical array circuit back to the mainline programmable logic array circuit at the point where it was suspended. By nesting programmable logic array circuits many functions can take place.

Publication No. EP 377976 A3 (Update 199347 E)
Publication Date: 19930127
Assignee: IBM CORP (IBMC)
Inventor: CONCHA F
LOFFREDO J M
Language: EN
Application: EP 1989313061 A 19891213 (Local application)
Priority: US 1989296168 A 19890112
Original IPC: B06F-9/22(B) G06F-1/00(B) G06F-9/22(B)
Current IPC: B06F-9/22(B) G06F-1/00(B) G06F-9/22(B)
Claim: The control apparatus uses program logic array circuits. A firmware structure containing a mainline programmable logic array circuit may be used to provide for efficient use of computer micro-codes. As the states of the mainline logic array are sequenced, the data bits representing the encode number field in its OR array are compared with the data bits representing the encode number field of the AND array of the subroutine programmable logic array circuit.
If a match is made, the mainline programmable logic array circuit suspends its operation and sequencing of the subroutine logical array circuit begins in order to perform the function required. Upon completion of the function, control is automatically transferred from the subroutine logical array circuit back to the mainline programmable logic array circuit at the point where it was suspended. By nesting programmable logic array circuits many functions can take place.
Publication No. EP 377976 B1 (Update 199633 E)
Publication Date: 19960717
**Mikroprogrammierte Steuervorrichtung mit programmierbaren logischen Anordnungen
Microcode control apparatus utilizing programmable logic array circuits
Dispositif de commande microprogramme utilisant des circuits a reseaux logiques programmables**
Assignee: International Business Machines Corporation, Old Orchard Road, Armonk, N.Y. 10504, US (IBMC)
Inventor: Concha, Fernando, 9604 Saddlebrook Drive, Boca Raton Florida 33496, US
Loffredo, John Mario, 2694 S.W. 14th Drive, Deerfield Beach Florida 33442, US
Agent: Burt, Roger James, Dr., IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, GB
Language: EN (16 pages, 6 drawings)
Application: EP 1989313061 A 19891213 (Local application)
Priority: US 1989296168 A 19890112
Designated States: (Regional Original) DE FR GB

Original IPC: G06F-9/22(A)
Current IPC: G06F-9/22(A)

Claim: 1. Eine mikroprogrammierte Steuervorrichtung fuer einen Rechner, wobei die Mikrowoerter benutzt werden, um die Rechnerbefehle auszufuehren und die Vorrichtung enthaelt: einen ersten PLA (34) mit einer Eingabepartitionierung, die eine Vielzahl von Status enthaelt, um einen Operationsschluessel von einem Rechnerbefehl zu empfangen, Sequentialisierungsmittel (38), um die Status der Eingabepartitionierung zu inkrementieren und eine Ausgabepartitionierung zur Generierung von Ausgabesaetzen mit Datenbits (42, 48, CP), welche der Anzahl von Status entspricht, die in der Eingabepartitionierung vorhanden ist; mindestens einen zweiten PLA (36) mit einer Eingabepartitionierung, die eine Vielzahl von Status enthaelt, um einen Satz Datenbits aus der Ausgabepartitionierung des ersten PLA (34) zu empfangen, Sequentialisierungsmittel (40), um die Status der Eingabepartionierung zu inkrementieren, und eine Ausgabepartitionierung zur Generierung der Ausgabesaetze mit Datenbits, welche der Anzahl von Status entsprechen, die in der Eingabepartitionierung vorhanden sind; wobei mindestens ein zuvor definierter Teil (48) der Ausgabesaetze mit Datenbits des ersten PLA (34) als Eingabe in die Eingabepartitionierung des zweiten PLA (36) bereitgestellt wird, wobei der zweite PLA (36) so angeordnet ist, dass dessen Funktion aufgerufen wird, wenn der zuvor definierte Teil der Ausgabesaetze mit Datenbits des ersten PLA (34) einer zuvor definierten Codenummer entspricht, die Ausgabepartitionierung des zweiten PLA (36) mindestens ein Steuersignal liefert, das einem Mikrowort entspricht, um eine Funktion auszufuehren, die von dem Operationsschluessel verlangt wird, durch ein ODER-Gatter (43) gekennzeichnet ist, das direkt mit den jeweiligen Ausgabeteilen der ersten und zweiten PLA verbunden und angeordnet ist, um die Sequentialisierungsmittel (38) des ersten PLA (34) zu inkrementieren, wenn mindestens einer der Ausgabebits (44) des zweiten PLA (36) oder mindestens ein Bit der Ausgabe (42) des ersten PLA (34) in einem der zuvor bestimmten zwei Werte liegt, und in dem ein anderer der Ausgabebits (46) des zweiten PLA (36) wirksam ist, um die Sequentialisierungsmittel (40) des zweiten PLA (36) in einem der zuvor bestimmten zwei Werte zu inkrementieren,

* die Ausgabestatus des ersten PLA (34) so sind, dass deren Ausgabe nicht wirksam ist, um den ersten PLA (34) zu inkrementieren, wenn der zuvor definierte Teil der Saetze mit Datenbits in der Ausgabepartitionierung des ersten PLA (34) der zuvor definierten Codenummer entspricht, und die Ausgabestatus des zweiten PLA (36) so sind, dass unmittelbar nach dem Aufruf der zweite PLA (36) funktionsfaehig bleibt, bis dessen Ausgabe effektiv ist, damit diese nicht laenger inkrementiert wird (46), bis diese auf dem einen Wert ist und so wird deren andere Ausgabe (44), die wirksam ist, um den ersten PLA (34) zu inkrementieren, danach zu dem einzigen Wert, um die Inkrementierung der ersten PLA (34) durchzufuehren, wobei daraus eine automatische Rueckfuehrung in den ersten PLA (34) aus dem zweiten PLA (36) resultiert.

1. A microcode control apparatus for a data processor wherein microwords are used to effect execution of processor instructions, the apparatus comprising: a first PLA (34) having an input partition containing a plurality of states for receiving an operation code of a processor instruction, sequencing means (38) for incrementing the

states of the input partition, and an output partition for generating output sets of data bits (42, 48, CP) corresponding to the number of states present in the input partition; at least a second PLA (36) having an input partition containing a plurality of states for receiving a set of data bits from the output partition of the first PLA (34), sequencing means (40) for incrementing the states of the input partition, and an output partition for generating output sets of data bits corresponding to the number of states present in the input partition; wherein at least a predefined portion (48) of the output sets of data bits of the first PLA (34) is provided as input to the input partition of the second PLA (36), the second PLA (36) being arranged so that operation thereof is initiated when said predefined portion of the output sets of data bits of the first PLA (34) corresponds to a predefined encode number, the output partition of the second PLA (36) providing at least one control signal, corresponding to a microword, for effecting a function required by the operation code, characterised by an OR gate (43) directly connected to respective output portions (42, 44) of the first and second PLAs and arranged to increment the sequencing means (38) of the first PLA (34) when either at least one of the output bits (44) of the second PLA (36) or at least one bit of the output (42) of the first PLA (34) is at a predetermined one of two values, and in that another of the output bits (46) of the second PLA (36) is effective to increment the sequencing means (40) of the second PLA (36) at a predetermined one of two values,

* the output states of the first PLA (34) being such that the output thereof is not effective to increment the first PLA (34) when the predefined portion of the sets of data bits in the output partition of the first PLA (34) corresponds to the predefined encode number and the output states of the second PLA (36) being such that once initiated the second PLA (36) remains operative until the output thereof effective to increment it no longer (46) is at the one value and so that the other output thereof (44) effective to increment the first PLA (34) is thereafter at the one value for effecting incrementation of the first PLA (34), an automatic branching back to the first PLA (34) from the second PLA (36) resulting therefrom.

United States
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PLA microcode controller
Assignee: International Business Machines Corporation
Inventor: Concha, Fernando, FL, US
Loffredo, John M.
Agent: Bogdon, Bernard D.
Language: EN
Application: US 1989296168 A 19890112 (Local application)
Original IPC: G06F-1/00
Current IPC: G06F-1/00(A)
Original US Class (main): 395775
Original US Class (secondary): 364DIG.001 364DIG.002 364244 364244.9 364259 364259.1 364261.3 364262 364262.4 364262.5 364262.8 364927.8 364933 364933.7 364938 364938.3 364942.7 364946.2 364946.6 364946.9 364948.3 364965 364965.5 364965.77